DERWENT-ACC-NO: 2002-009101
DERWENT-WEEK: 200201
COPYRIGHT 1999 DERWENT INFORMATION LTD

TITLE: Method for producing N-type MOS transistor - not only can reduce the PN junction leakage of the NMOS transistor, but also alleviate the short channel effect

INVENTOR: LIN, B; WANG, J ; WU, C

PATENT-ASSIGNEE: TAIWAN SEMICONDUCTOR MFG CO LTD[TASEN]

PRIORITY-DATA: 1999TW-0113164 (August 2, 1999)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
TW 434705 A	May 16, 2001	N/A	000	H01L 021/28

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
TW 434705A	N/A	1999TW-0113164	August 2, 1999

INT-CL_(IPC): H01L021/28

ABSTRACTED-PUB-NO: TW 434705A

BASIC-ABSTRACT: NOVELTY - The present invention provides a method for producing an N-type MOS transistor, which comprises: providing a semiconductor substrate formed with a gate electrode and a gate oxide layer; implanting indium ions to form a pocket ion doped region on the semiconductor substrate below the gate electrode, meanwhile the semiconductor substrate between the pocket ion doped region and said gate oxide layer has a defect; implanting N-type ions on the semiconductor substrate below both sides of the gate electrode to form a lightly doped region of source/drain; secondly, without going through a rapid thermal annealing, directly form a spacer on the sidewall of the gate electrode; and implanting N-type ions on the semiconductor

substrate below both
sides of the gate electrode to form a heavily doped region of source/drain.
The method according to the present invention not only can reduce the PN
junction leakage of the NMOS transistor, but also can alleviate the short
channel effect.

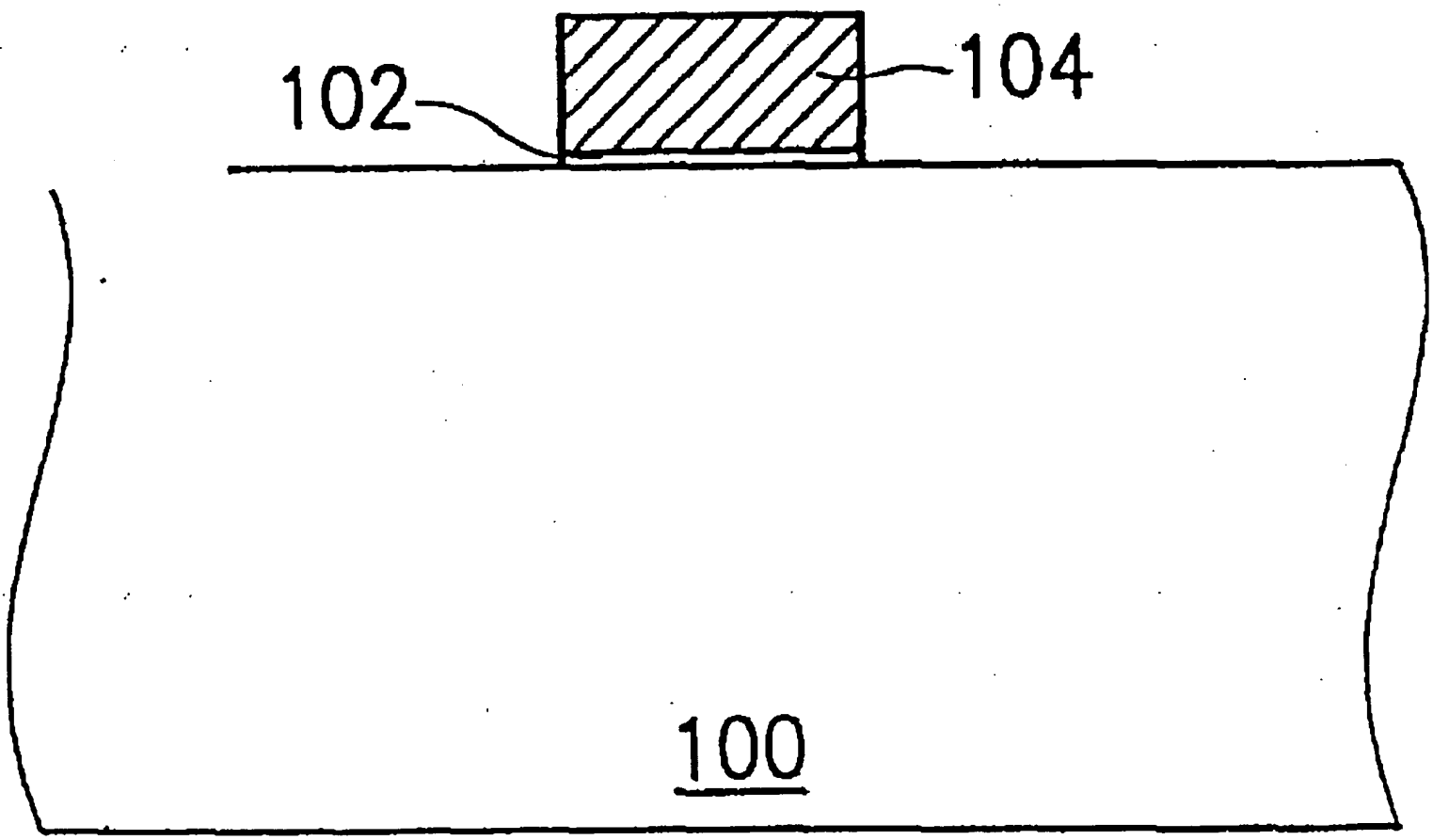
CHOSEN-DRAWING: Dwg.1/1

TITLE-TERMS:
METHOD PRODUCE N TYPE MOS TRANSISTOR CAN REDUCE PN JUNCTION LEAK NMOS
TRANSISTOR ALLEVIATE SHORT CHANNEL EFFECT

DERWENT-CLASS: U11 U12

EPI-CODES: U11-C18A3; U12-D02A;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N2002-007544


102
104
100